CLAIMS

What is claimed is:

1. A multiplier circuit, comprising:

at least one Booth encoder circuit to encode a plurality of multiplier bits into four encoded outputs, the encoded outputs to select Booth-multiply functions; and

a plurality of multiplexer circuits, one multiplexer circuit for each bit of the multiplicand, at least one of the plurality multiplexer circuits including four pass gates coupled to receive a multiplicand bit, a complement of the multiplicand bit, multiplexed data from a next lower order multiplexer circuit and the encoded outputs of the Booth encoder circuit to provide one bit of a partial product at a multiplexer output.

2. The multiplier circuit of claim 1, wherein the four encoded outputs select Booth-multiply functions which include negative, positive, zero, multiply by one and multiply by two.

3. The multiplier circuit of claim 1, wherein the multiplier circuit includes M/2 Booth encoder circuits each coupled to a plurality of multiplexer circuits, each Booth encoder circuit receiving three bits of an M-bit multiplier to output M/2 Booth-multiply partial products.

4. The multiplier circuit of claim 3, wherein the multiplier circuit further includes an adder circuit coupled to the outputs of the multiplexers to add the partial products and obtain a product of the multiply operation.

5. The multiplier circuit of claim 3 further including a N-bit multiplicand, wherein M and N are integers selectable from one or a combination of sixteen, thirty-two and sixty-four.

6. The multiplier of claim 1, wherein the Booth encoder circuit includes at least one fanout driver circuit to drive at least one select output and the outputs of the multiplexer circuits include fanout drivers to drive the partial product bits.

7. The multiplier circuit of claim 6, wherein the fanout drivers include inverters.

8. A plurality of multiplexer circuits, each multiplexer circuit including four transistors, the transistors coupled to receive Booth encoded signals, a multiplicand bit, a complement of the multiplicand bit, and at least one of the multiplexer circuits coupled to receive multiplexed data from a next lower order multiplexer circuit, wherein one bit of a partial product is selected for output from the at least one multiplexer circuit according to the Booth encoded signals.

9. The circuit of claim 8, wherein the four transistors include:

first and second transistors, the gates of the transistors coupled to receive a multiplicand bit and its complement, a first source/drain region of the transistors coupled to receive first and second Booth encoded signals and a second source/drain region of the transistors coupled together and coupled to the input of a next higher order multiplexer, the coupled second source/drain regions to provide a positive or a negative multiplicand bit according to the first and second Booth encoded signals; and

a third transistor, a first source/drain region of the third transistor coupled to the second source/drain regions of the first and second transistors, the gate of the third transistor coupled to receive a third Booth encoded signal, and a second source/drain region of the third transistor providing an output corresponding to one bit of a partial product; and

a fourth transistor, a first source/drain region of the fourth transistor to receive multiplexed data from a next lower order multiplexer; the gate of the fourth transistor to receive a fourth Booth encoded signal, a second source/drain region of

the fourth transistor coupled to the second source/drain region of the third transistor, the coupled second source/drain regions to provide one bit of a partial product according to the third and fourth Booth encoded signals.

10. The circuit of claim 8, wherein the Booth encoded signals include four Booth encoded signals encoded from three bits of a multiplier and which select Booth-multiply functions that include negative, positive, multiply by two and multiply by one.

11. The circuit of claim 10, wherein a multiplexer output is zero when both the positive and negative result signals are low.

12. The circuit of claim 8, wherein a delay from a multiplicand bit to an output of the circuit is a maximum of two transistor delays.

13. The circuit of claim 8, wherein the transistors include NFET transistors.

14. A Booth encoder circuit comprising:

a plurality of logic circuits to generate control signals used to generate Booth-multiply partial products, the logic circuits only including:

a first logic circuit to generate a signal for a negative partial product;

a second logic circuit to generate a signal for a positive partial product;

a third logic circuit to generate a signal to multiply a multiplicand by two; and

a fourth logic circuit to generate a signal to multiply a multiplicand by one.

15. The circuit of claim 14, wherein the Booth encoder circuit generates a zero partial product when outputs of the first and second logic circuits are both low.

16. The circuit of claim 14, wherein inputs to the logic circuits include bits of a multiplier and complements of the bits of a multiplier.

17. The circuit of claim 16, wherein the first logic circuit comprises:

a two-input NAND gate, wherein the inputs to the NAND gate are first and second bits of a multiplier;

a T-gate coupled to the output of the NAND gate, wherein a third multiplier bit and a complement of the third multiplier bit activate the T-gate, and wherein the output of the T-gate includes the signal for a negative partial product; and

a pull-down transistor coupled to the output T-gate, wherein the complement of the third multiplier bit activates the pull down transistor.

18. The circuit of claim 16, wherein the first logic circuit comprises:

a fifth logic circuit that is high when first, second and third bits of a multiplier are not all ones or all zeros; and

a two-input AND gate, wherein a first input to the AND gate is the output of the fifth logic circuit and a second input is the third bit of a multiplier.

19. The circuit of claim 16, wherein the second logic circuit comprises:

a two-input NAND gate, wherein the inputs to the NAND gate are complements of first and second bits of a multiplier;

a T-gate coupled to the output of the NAND gate, wherein a third multiplier bit and a complement of the third multiplier bit activate the T-gate, and wherein the output of the T-gate includes a signal for the positive partial product; and

a pull-down transistor coupled to the output T-gate, wherein the third multiplier bit activates the pull down transistor.

20. The circuit of claim 16, wherein the second logic circuit comprises:

a fifth logic circuit that is high when first, second and third bits of a multiplier are not all ones or all zeros; and

a two-input AND gate, wherein a first input to the AND gate is the output of the fifth logic circuit and a second input is a complement of the third bit of a multiplier.

21. The circuit of claim 16, wherein the third logic circuit comprises a two-input XOR gate, wherein the inputs to the XOR gate are first and second bits of a multiplier and the output of the XOR gate is the signal to multiply a multiplicand by one.

22. The circuit of claim 16, wherein the fourth logic circuit comprises a two-input XNOR gate, wherein the inputs to the XNOR gate are first and second bits of a multiplier and the output of the XNOR gate is the signal to multiply a multiplicand by two.

23. A method of multiplying comprising:

generating four control signals to implement Booth encoding functions of negative, positive, zero, multiply by one and multiply by two, from bits of a multiplier;

multiplexing bits of a multiplicand in accordance with the control signal functions to generate partial products, wherein multiplexing includes interconnecting intermediate stages of multiplexers from lower order bit positions to next higher order positions; and

adding the partial products to obtain the final product.

24. The method of claim 23, wherein multiplexing includes distributing the multiplicand bits to create a maximum delay of two transistors from a multiplicand bit to an output of the circuit.

25. The method of claim 23, wherein generating control signals includes generating the zero function signal when the negative and positive function signals are both low.

26. The method of claim 23, wherein multiplexing to generate partial products includes simultaneously generating M/2 partial products for an M-bit multiplier.

27. The method of claim 23, wherein multiplexing to generate partial products includes generating one partial product, and adding includes accumulating a sum of the partial products as the partial products are generated.

28. A computer system comprising:

a bus that communicates information;

a memory coupled to the bus, the memory to store a multiply instruction; and

a processor coupled to the bus, the processor to process information, the processor including a multiplier circuit, the multiplier circuit including at least one partial product generator, wherein the at least one partial product generator includes:

a Booth encoder circuit to encode a plurality of multiplier bits into four encoded outputs, the encoded outputs to select Booth-multiply functions; and

a plurality of multiplexer circuits, one multiplexer circuit for each bit of the multiplicand, at least one of the plurality of multiplexer circuits including:

four pass gates, the pass gates coupled to a multiplicand bit, a complement of the multiplicand bit, multiplexed data from a next lower order multiplexer circuit and the Booth encoder circuit outputs, the Booth encoder circuit outputs to enable one or a combination of the pass gates to provide one bit of a partial product at a multiplexer output.

29. The computer system of claim 28, wherein the Booth encoder select outputs to enable the functions positive, negative, zero, multiply by one and multiply by two.

30. The computer system of claim 29, wherein the multiplier circuit implements a sixty-four by sixty-four bit multiply.